## REMARKS

In the last Office Action, the Examiner rejected claims 4-6 under 35 U.S.C. §102(e) as being anticipated by Ohsawa (US 2002/0051378). Claim 2 was rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,713,325. Claim 3 was rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,713,325 in view of Ohsawa. Additional art was cited of interest.

In accordance with the present response, independent claim 4 has been amended to further patentably distinguish from the prior art of record. As discussed in detail below, the prior art of record does not disclose or suggest a semiconductor integrated circuit having a source region and a drain region having source extension regions and drain extension regions, respectively, stacked in the thickness direction of a semiconductor film.

Applicants request reconsideration of their application in light of the foregoing amendment and the following discussion.

## Double Patenting Rejections

The present application is a division of parent application Serial No. 10/267,365, now U.S. Patent No. 6,713,325, and has been filed as a consequence of a restriction requirement made in the parent application. All of the claims in the present application are directed to species restricted out of the parent application pursuant to the restriction requirement. Under 35 U.S.C. §121, U.S. Patent No. 6,713,325 which issued on the parent application "shall not be used as a reference...against a divisional application." Therefore the nonstatutory double patenting rejections were made in error and should be withdrawn.

In the event the double patenting rejections are not withdrawn, a terminal disclaimer is submitted herewith disclaiming the terminal part of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 6,713,325. Also submitted is the required statutory disclaimer fee. Applicants request that the terminal disclaimer not be entered if, on reconsideration, the Examiner withdraws the double patenting rejections as requested in the preceding paragraph.

The filing of the terminal disclaimer, as noted by the Examiner, overcomes the obviousness-type double patenting rejections, thereby placing claims 2-3 in allowable form.

## Brief Summary of Invention

With reference to the embodiment shown in Figs. 1A-2F and 3A-3B, the present invention relates to a semiconductor integrated circuit in which a CMOS transistor is formed on a first conductivity type semiconductor film 1 provided on a first conductivity type supporting substrate 3 through an embedded insulating film 2. A second conductivity type source region 15 and a second conductivity type drain region 14 formed in the semiconductor film 1. A gate insulating film 13 is formed on an upper surface of the semiconductor film 1. A gate electrode 12 formed on an upper surface of the gate insulating film 13.

According to the present invention, the source region 15 includes an ultra-shallow high-density N-type source extension region 141 at a boundary with a channel region, a low-density N-type source extension region 142 under the ultra-shallow high-density N-type source extension region 141, and an embedded insulating neighboring N-type source extension region 143, the source extension regions 141-143 being stacked in a thickness direction of the semiconductor film 1. The drain region 14 includes an ultra-shallow high-density N-type drain extension region 151 at a boundary with the channel region, a low-density N-type drain extension region 152 under

the ultra-shallow high-density N-type drain extension region 151, and an embedded insulating neighboring N-type extension drain region 153, the drain extension regions 151-153 being stacked in a thickness direction of the semiconductor film 1.

By the foregoing construction, N-type impurity regions where only parts of the source and drain regions have a low density can be formed. As a result, the electric potential concentration in the vicinity of a surface proximate the drain and in the vicinity of the insulating film can be reduced, thereby reducing the generation of impact ions.

## Traversal of Prior Art Rejection

Claims 4-6 were rejected under 35 U.S.C. §102(e) as being anticipated by Ohsawa. Applicants respectfully traverse this rejection and submit that claims 4-6 recite subject matter which is not identically disclosed or described in Ohsawa.

**Independent Claim 4**

Amended independent claim 4 is directed to a semiconductor integrated circuit in which a CMOS transistor is formed on a first conductivity type semiconductor film provided on a first conductivity type supporting substrate through an embedded insulating film. Claim 4 requires a second conductivity type source region and a second conductivity type drain region formed in the semiconductor

film, a gate insulating film formed on an upper surface of the semiconductor film, and a gate electrode formed on an upper surface of the gate insulating film. Amended claim 4 further requires that the source region includes an ultra-shallow high-density N-type source extension region at a boundary with a channel region, a low-density N-type source extension region under the ultra-shallow high-density N-type source extension region, and an embedded insulating neighboring N-type source extension region, the source extension regions being stacked in a thickness direction of the semiconductor film. Amended claim 4 further requires that the drain region includes an ultra-shallow high-density N-type drain extension region at a boundary with the channel region, a low-density N-type drain extension region under the ultra-shallow high-density N-type drain extension region, and an embedded insulating neighboring N-type extension drain region, the drain extension regions being stacked in a thickness direction of the semiconductor film.

Thus amended claim 4 requires a source region having source extension regions stacked in a thickness direction of the semiconductor film, and a drain region having drain extension regions stacked in a thickness direction of the semiconductor film. No corresponding structural arrangement is disclosed or described by Ohsawa. More specifically, in the semiconductor memory device shown in Fig. 49 of Ohsawa,

drain regions 14a, 14b are stacked or extend along a length, not a thickness, direction of an insulating film 11. Likewise, source regions 15a, 15b shown in Fig. 49 of Ohsawa are stacked or extend along a length, not a thickness, direction of an insulating film 11.

**Independent Claim 6**

With reference to the embodiment shown in Figs. 11A-13B, independent claim 6 is directed to a semiconductor integrated circuit in which a CMOS transistor is formed on a first conductivity type semiconductor film 1 provided on a first conductivity type supporting substrate 3 through an embedded insulating film 2. Claim 6 requires a second conductivity type source region 144 and a second conductivity type drain region 154 formed in the semiconductor film, a gate insulating film 11 formed on an upper surface of the semiconductor film 1, and a gate electrode 12 formed on an upper surface of the gate insulating film 11. Claim 6 further requires that a channel region disposed under the gate insulating film 12 has a first conductivity type impurity region 22 having a higher density than a well 7 at a boundary with the drain region 154. No corresponding structural combination is disclosed or described by Ohsawa.

The semiconductor memory device shown in Fig. 40 of Ohsawa has a bulk region 12b and a channel region portion 12a corresponding to the well 7 and the impurity region 22,

respectively, of the invention recited in claim 6. Ohsawa discloses that the portion 12a of the channel region has a lower density (i.e, a lower boron concentration) than the bulk region 12b (see paragraph [0289] in Ohsawa). In contrast, claim 6 explicitly recites that the first conductivity impurity region (i.e., corresponding to the portion 12a in Ohsawa) has a higher density than the well (i.e., corresponding to the bulk region 12b in Ohsawa) at the boundary with the drain region.

In the absence of the foregoing disclosure recited in amended independent claim 4 and independent claim 6, anticipation cannot be found. See, e.g., W.L. Gore & Associates v. Garlock, Inc., 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984) ("Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration"); Continental Can Co. USA v. Monsanto Co., 20 USPQ2d 1746, 1748 (Fed. Cir. 1991) ("When more than one reference is required to establish unpatentability of the claimed invention anticipation under § 102 can not be found"); Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984) (emphasis added) ("Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim").

Stated otherwise, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. This standard is clearly not satisfied by Ohsawa for the reasons stated above. Furthermore, Ohsawa does not suggest the claimed subject matter and, therefore, would not have motivated one skilled in the art to modify Ohsawa's semiconductor memory device to arrive at the claimed invention.

Claim 5 depends on and contains all of the limitations of amended independent claim 4 and, therefore, distinguishes from Ohsawa at least in the same manner as amended claim 4.

In view of the foregoing amendments and discussion, the application is believed to be in allowable form. Accordingly, favorable reconsideration and allowance of the claims are most respectfully requested.

Respectfully submitted,

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